IN THE SPECIFICATION

Please replace the paragraph beginning at page 60, line 2, with the following rewritten paragraph:

FIG. 29 shows a circuit which solves the above-mentioned problem and realizes VCLK signal generation and pixel clock generation at the same time. A description will now be given below, with reference to FIG. 29, of an operation. In the circuit shown in FIG. 29, the ~~VLCK~~ VCLK signal is generated by a PLL loop PLL comprising: a phase frequency comparison circuit 1322 which compares a reference clock and a result of N division of the ~~VLCK~~ VCLK signal by a programmable counter 1321; a loop filter 1323 which filters a result of the phase frequency comparison circuit 1322; and a VCO 1324 of which oscillation frequency changes in response to an output voltage of the loop filter 1323. Additionally, the dividing ratio N of the programmable counter 1321 is set by an external frequency dividing ratio setting.

Please replace the paragraph beginning at page 60, line 17, with the following rewritten paragraph:

Thus, the VCLK signal is generated, and the pixel clock synchronous with a phase synchronous pulse is generated at a frequency of 1/8 of the ~~VLCK~~ VCLK signal by loading data=0 from a load pulse generator 1325 to a 1/8 frequency dividing circuit by the VCLK signal and the phase synchronous signal.

Please replace the paragraph beginning at page 61, line 15, with the following rewritten paragraph:

Furthermore, in the present embodiment, the count (frequency dividing) of the 1/8 frequency dividing circuits 1326 and 1327 can be enabled/disabled by a Phase-Set signal. In

the case of the present embodiment, a rising edge of the Phase-Set signal is caught by VCLK so as to stop a counting (frequency dividing) operation for one clock cycle of VCLK. ~~By doing this was~~ Consequently, the phase of the pixel clock and the internal clock can be delayed by 1/8 clock unit. By performing phase delay of 1/8 clock cycle at a predetermined interval (or close to a predetermined interval) during one scanning period, the frequency of the pixel clock during one scanning period can be finely controlled in an equivalent manner. This is equivalent to an ability to more finely set the frequency variable step, which can be set by PLL-LOOP.

Please replace the paragraph beginning at page 62, line 6, with the following rewritten paragraph:

Furthermore, when advancing by 1/8 clock, fine control can be achieved by reducing by 1/8 clock by loading data=1 instead of loading data=0 so as to change as frequency=~~8~~ 7, as shown in FIG. 30. At this time, if load data is set, the data is output from [[eth]] ~~the~~ register ~~11329~~ 1329 to the frequency dividing circuit 1326-1, and when the frequency dividing number=7 is output, it is shortened, and when the frequency dividing number=9 is output, it is prolonged.

Please replace the paragraph beginning at page 62, line 22, with the following rewritten paragraph:

In a case of a multi-beam optical system in which the light-emitting part of the semiconductor laser LD is constituted by a plurality of light-emitting parts, if each oscillation wavelength is different, a cause of image degradation is generated since a difference is generated in the scanning width of the scanning light by each light-emitting part by color aberration of a scanning optical system for scanning and forming an image on the surface to

be scanned, which causes a shift [[off]] of image position for each scanning line or an intensity fluctuation in a highlight part.

Please replace the paragraph beginning at page 63, line 8, with the following rewritten paragraph:

The difference of the scan width can be corrected by using the above-mentioned phase shift, and writing can be performed at a desired target writing position. A shift may be made to shorten the scan width which will be prolonged, and a shift may be made to prolong the scan width which will be shortened. On the other hand, when the original image clock is compressed beforehand so as to be relatively short, an amount of shift may be changed for each of the light-emitting parts of which scan width is prolonged and the light-emitting ~~part~~ parts of which scan width is shortened.